REMARKS

Claim Rejections – 35 U.S.C. § 103

Claims 1-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Curello in view of Taka et al. Favorable reconsideration of this rejection is respectfully requested.

Curello discusses how and in what order a semiconductor device is manufactured. The Office Action states that in regard to claim 1, Curello teaches either in the source or drain regions of the device that, "the second junction ('a drain 66') being deeper than the first junction ('a source 64')." The Office Action further contends that the "second junction ('a drain 66') overlapping '(produce some gate overlap)' with the first junction ('a source 64') with leaving a part of the first junction ('a source 64') existing under the gate ('gate oxide layer 42')." When Curello refers to the first and second junctions they are referring to the source and drain respectively, not two junctions within the same source or drain, as claim 1 of the present invention states:

> ...forming a second junction by doping an n-type impurity in the semiconductor region by using at least the gate as a mask, the second junction being deeper than the first junction, the second junction overlapping with the first junction with leaving a part of the first junction existing under the gate....

One reasonably skilled in the art would not believe that the source and drain regions of the present invention overlap, this would short out each region, source to drain. The reasonable interpretation would be that the overlapping of the junctions occurs in the same region; i.e. the source or the drain region. The "second junction," as stated in claim 1, refers to the second junction in the same region of either the source or the drain. Furthermore, Curello does not teach that a source or drain region

overlap each other. The Office Action only states that the drain region (66) and a source region (64), produce some overlap with the gate, but not with each other as previously cited in claim 1 of the present invention.

The Office Action uses Taka in an attempt to show that the present method of double implantation, first at a low energy and high dose, and second at a high energy and low dose, would have been obvious, thereby negating the latter elements of claim 1 of the present invention. Described in the preferred embodiment section of Taka, is how to form an n-well using a multiple implantation method. The Office Action cites lines 39-44 of column 3, and lines 7-11 of column 4, to show that in forming the n-well, the first implantation is at lower energy, higher dose, and the second implantation is at higher energy, lower dose. The Office Action did not address the fact that the n-well regions referred to are different. The first implantation refers to region 22 of figure 1D while the second implantation refers to regions 26-1 and 26-2 of figure 2C, two separate and distinct regions of the semiconductor. Therefore Taka does not disclose what is taught in the present invention.

In Taka, for manufacturing a bipolar transistor, an N+ buried region is formed on a surface of a semiconductor substrate firstly by the first ion-implantation. Next, a polycrystalline silicon film is formed on the surface of the substrate and is patterned. Thereafter, the polycrystalline silicon film is covered with a silicon oxide film and, by dry etching, the surface of the substrate is in a condition of

being covered with the polycrystalline silicon film and the silicon oxide film. In this condition, the second ion-implantation and so on are performed.

In contrast, in the present invention, as described in Fig. 1B and its description of the present application, to obtain an impurity distribution of Fig. 1B on a source/drain, both the first and second ion-implantations are performed to a surface of the semiconductor region (semiconductor substrate). When the first ion-implantation and the second ion-implantation are carried out to the different surfaces as in Taka, it is of course impossible to obtain the impurity distribution of Fig. 1B. Accordingly, it is not possible to achieve an object of the invention of the present application.

That is, in the invention of the present application, an ion-implantation is carried out to the surface of the substrate while, in Taka, the ion-implantation is carried out to the surface of the substrate on which the polycrystalline silicon film or the silicon oxide film is formed. In Taka, even if a process such as removing a film in the surface is carried out after the ion-implantation, it is extremely difficult to operate a MOS transistor having a short gate length while reducing the junction leak current, which is the object of the invention of the present application. Even though it is achieved, it is very inefficient.

The Office Action states that Curello discloses forming a shallow source and drain, but there is no such description in Curello. Accordingly, it is very hard to conceive the invention of the

present application however Curello and Taka are combined. Therefore, the invention of the present application is not obvious.

Conclusion

In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Office Action believes that this application is not now in condition for allowance, the Office Action is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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